WHAT IS CLAIMED IS:

1. A Fast Fourier Transforming apparatus for compensating an OFDM output bit signal, comprising:

an input buffer unit for storing and outputting a received OFDM bit signal;

a butterfly operation unit for performing a butterfly operation according to a radix algorithm at each stage;

a scale detection unit for calculating and outputting a scale factor which is a division factor used for controlling a bit value of a butterfly operated signal input from the butterfly operation unit to the input buffer unit at each stage within a predetermined bit limit of the received OFDM signal,

a scale count unit for cumulative counting a count coefficient corresponding to the scale factor input from the scale detection unit, and then outputting the result, and

a compensation unit for controlling the bit of a signal input from the butterfly operation unit according to values obtained from the scale detection unit and the scale count unit, and then outputting the result.

2. The Fast Fourier Transforming apparatus of claim 1, further comprising a first operation unit for dividing a bit value of a later input signal by the scale factor and outputting the result, thereby considering the scale factor from the scale detection unit when performing the butterfly operation.

3. The Fast Fourier Transforming apparatus of claim 1, further comprising an output buffer unit for storing a signal output from the butterfly

operation unit at each of the stages and a control unit for controlling the signal stored in the output buffer unit to feed back to the input buffer unit until the butterfly operation is conducted as many times as the predetermined number of stages and outputting a butterfly operated signal at a final stage of the predetermined stages to the bit compensating unit.

4. The Fast Fourier Transforming apparatus of claim 3, wherein a radix-2 algorithm is applied to the butterfly operation unit, the control unit controls the OFDM bit signal to be input to the input buffer unit by units of **8** bits and controls the predetermined bit limit of the scale detection unit to be set to **12** bits.

5. The Fast Fourier Transforming apparatus of claim 4, wherein the scale factor is to be set to **4** if an absolute value of the butterfly operated bit signal is more than **1024**, to **2** if **512** and to **1** if **256** so that the butterfly operated bit value can be maintained at **8** bits.

6. The Fast Fourier Transforming apparatus of claim 5, wherein the scale count unit applies **4** as the count figures if the scale factor from the scale detection unit is **4, 2** if **2** and **1** if **0** for cumulative counting the count figures corresponding to the scale factor.

7. The Fast Fourier Transforming apparatus of claim 1, wherein the compensation unit compensates for the bit value of the input signal of the input buffer unit by the difference of the bit value of the predetermined number of stages and the input signal to the scale count unit.

8. The Fast Fourier Transforming apparatus of claim 7, wherein the compensation unit comprises,

a second operation unit for dividing the bit value of the butterfly operated output signal at the final stage of the predetermined stages by the scale factor calculated at the final stage,

a division and multiplication selection unit for calculating a difference value of the predetermined number of stages and an output value from the scale count unit, comparing the predetermined number of stages with the output value from the scale count unit and outputting a selection data for division operation if the predetermined number of stages is greater or a selection signal for multiplication if the output value from the scale count unit is greater,

a factor calculation unit for calculating and outputting a quotient **Q** and a remainder **R** by dividing the difference value by **2**,

a division and multiplication calculation unit for dividing the value output from the second operation unit by 2^{Q} if the selection data is for the division operation while for multiplying the value output from the second operation unit by 2^{Q} if the selection data is for the multiplication operation,

a bit compensation unit for compensating the value output from the division and multiplication calculation unit according to the selection data from the division and multiplication selection unit and the remainder **R** from the coefficient calculation unit, and